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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/785,648	02/24/2004	Timothy A. Rost	TI-36595	3709

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EXAMINER	
PHAM, LONG	
ART UNIT	PAPER NUMBER
2814	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/785,648	ROST, TIMOTHY A.	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

New grounds of rejection

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 9-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ouyang et al. (US publication 2004/0256639) in combination with Lin et al. (US publication 2005/0035369), Yeo et al. (US publication 2005/009263), Chidambarrao et al. (US publication 2005/0164477), and Currie et al. (US publication 2004/0173812).

With respell to claim 9, Ouyang et al. teach a method of fabricating a semiconductor device comprising (see [0028] and [0083]):

forming a PMOS devices on a semiconductor substrate with source to drain channel regions along a first crystallographic orientation axis of the semiconductor substrate;

forming a NMOS devices on the semiconductor substrate with source to drain channel regions rotated by an offset angle from the source lo drain channel regions of the PMOS devices lie along a second crystallographic orientation axis of the semiconductor substrate;

applying a compressive strain longitudinally across the source to drain channel regions of the PMOS devices to improve hole mobility; and

applying a tensile strain longitudinally across the source to drain channel regions of the NMOS devices to improve electron mobility.

Further with respect to claim 9, Quayang et al fail to teach forming lateral PMOS and NMOS or source, drain, and channel of the PMOS and NMOS within the substrate.

Lin et al. teaches forming lateral PMOS and NMOS or source, drain, and channel of the PMOS and NMOS within the substrate in which the channel is

strained to achieve both increased mobility (due to the straining of the channel) and size reduction (due to the lateral formation of PMOS and NMOS). See paras [0004] and [0011].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Lin et al. into the method of Ouyang et al. to attain the above advantage.

With respect to claim 10, Ouyang et al. further teach that the crystallographic orientation axis on which the PMOS devices are formed is <110> and wherein the semiconductor substrate is silicon (see [0040]).

With respect to claim 11, Ouyang et al. further teach that the crystallographic orientation axis on which the NMOS devices are formed is < 100 >.

With respect to claim 12, Ouyang et al. appear to teach the offset angle for the channel region of NMOS. See [0049].

Alternatively, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value for the angle between channel region of NMOS devices and channel region of PMOS devices through routine experimentation and optimization to obtain optimal or desired device performance because it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

With respect to claim 13, Ouyang et al. teach applying compressive strain to channel regions of PMOS devices but fail to teach the strain is uniaxial.

Lin et al. teach applying uniaxial compressive strain to improve hole mobility. See [0010].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Lin et al. into the method of Ouyang et al. to attain the above advantage.

With respect to claim 14, Ouyang et al. teach applying compressive strain to channel regions of PMOS devices but fail to teach the strain is biaxial.

Yeo et al. teach applying biaxial compressive strain to enhance hole mobility. See [0005].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Yeo et al. into the method of Ouyang et al. to attain the above advantage.

With respect to claim 15, Ouyang et al. teach applying compressive strain to channel regions of PMOS devices but fail to teach the application is done by recess etching and deposition of silicon-germanium epitaxial layer on the channel regions.

Yeo et al. teach applying compressive strain to the channel regions by recess etching and deposition of silicon-germanium epitaxial layer on the channel regions. See figs. 1-9 and associated text.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Yeo et al. into the method of Ouyang et al. to enhance carrier mobility. See [0008].

With respect to claim 16, Ouyang et al. teach applying tensile strain to the channel regions of NMOS devices but fail to teach the strain is biaxial.

Chidambarrao et al. teach applying biaxial tensile strain to channel regions to enhance mobility. See [0004].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Chidambarrao et al. into the method of Ouyang et al. to attain the above advantage.

With respect to claim 17, Ouyang et al. teach applying tensile strain to channel regions of NMOS devices but fail to teach the application is done by recess etching and deposition of carbon doped silicon layer on the channel regions.

Currie e al. teach applying tensile strain to the channel regions by recess

etching and deposition of carbon doped silicon layer on the channel regions. See [0077].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Currie et al. into the method of Ouyang el al. to improve device performance. See [0009].

With respect to claim 18, Ouyang et al. further leach forming an interlayer dielectric layer 68 over the NMOS device. See fig. 9.

Response to Arguments

Applicant's arguments with respect to claims 9-18 have been considered but are moot in view of the new ground(s) of rejection.

In response to the applicant's arguments in the paragraph bridging pages 5 and 6 of the response dated 12/26/06, it is submitted that the formation of lateral PMOS and NMOS or source, drain, and channel of the PMOS and NMOS within the substrate and having the channel strained would allow the dual benefits of size reduction (due to the lateral formation of PMOS and NMOS) and increased mobility (due to the straining of the channel).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Long Pham
Primary Examiner
Art Unit 2814

LP